Z100 IDE Interface and NVSRAM Board Design Description – Large Scale Design 3.0
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Introduction

The Z-100 LifeLine IDE Interface and NVSRAM design, hereafter referred to as the Z100 IDE Interface is a multifunction S-100 board designed for the Heath/Zenith Z-100 Series computer. It provides the following features:

- An interface from the Z-100 S-100 computer bus to the industry standard IDE hard drive interface. This allows you to connect to up to four standard IDE drives which are now much more available than the old MFM hard drives originally supported on the Z-100. DMA capabilities, however, are not supported. Solid state memory devices, such as compact flash cards, that use the IDE interface are also usable.

  The circuit design described here utilizes a complex programmable logic device (CPLD) from Altera for all of the control circuitry.

  Design Note: This programmable device was chosen because it would make development easier and the design hopefully more reliable and require less power. Altera was chosen because the development tools were readily available from their web site.

- A bootable NVsRAM device. This nonvolatile memory storage device, based on the Texas Instruments bq4850 programmable NVsRAM, can be programmed at any time without removing it from the board. The NVsRAM device is fully bootable and can contain up to 512k of user selectable programs or files, making it an excellent choice for holding the Z-DOS bootup files. The bq4850 has an onboard real time clock and an internal battery for memory retention. Therefore, no special programming voltage is required and programming is greatly simplified with no special timing routines required. Other models are available; see the schematic for a listing of devices thought to be compatible. Programming the real time clock is described in the software section.

- A breakout switch to enable program analysis using the Z-100's enhanced Monitor ROM utilities from the hand prompt or the DEBUG utility.

- A prototype area for adding your own options. One idea is to add a second NVsRAM chip selected by means of a toggle switch.

Theory of Operation

Main Schematic

Input Buffers

U1, 74LS245, provides buffering for the Data lines (DO0 through DO7) from the S-100 bus to the Interface board. U1 is enabled by the signal /IO_Write.

U2, 74LS244, provides buffering for the Data lines (DI0 through DI7) from the Interface board to the S-100 bus. U2 is enabled by the signal /IO_Read.

Address Decoding

The board is uniquely decoded at address 0080h through 008Fh by the Altera chip. S100 bus address lines A00 through A15 are routed to the Altera chip and these address lines are then decoded to only allow addresses 0080h through 008Fh to affect card operation.

This decoding could be changed but Altera chip reprogramming would be required.

Output Buffers

U9 and U12, both 74LS245s, buffer control and address signals to the IDE drive.

U7 and U8, both 74LS245s, buffer data to/from IDE J1.

U10 and U11, both 74LS245s, buffer data to/from IDE J2.

These buffers turned out to be very important to obtain reliable operation by providing the capability of turning the individual IDE connectors on and off under the Altera chip's control. The long IDE cables caused ringing and interaction without the buffers. Also note that all Control and Data lines have series termination resistors which help reduce ringing and improve overall bus transient response.

IDE Connector

J1 and J2 are the IDE connectors.

The following signal names are the IDE interface standard names for these signals and not necessarily the signal names on our card:

Pin	Name	Pin	Name
1	RESET	2	Gnd
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	Gnd	20	keypin
21	DMARQ (Not Used)	22	Gnd
23	WR/	24	Gnd
25	RD/	26	Gnd
27	IORDY (Not Used)	28	CSEL (Gnd)
29	DMACK (Not Used)	30	Gnd
31	INTRQ (Not Used)	32	Not Used
33	A1	34	PDIAG (used for detection between Master and Slave drives. No connect to IDE card.)
35	A0	36	A2
37	CS0	38	CS1
39	Drive LED (Not Used)	40	Gnd

A note about CSEL, Cable Select. Cable Select is a feature that most IDE drives have which allows two drives to be connected to a connector and not worry about which drive is connected as master and which as slave. This pin is grounded on the IDE card. It is pulled up by each IDE drive that supports CSEL. The selection is done on the IDE cable instead. CSEL is left unconnected on the connector farthest out from the computer. That makes that far end drive the Slave (Drive 1). The Master (Drive 0) is at the mid cable connector as it is pulled down to ground by the card. To use the CSEL feature you would have to either buy a special cable that supports it (may be difficult to find) or make your own by carefully finding and cutting the correct wire in the ribbon cable (also may be fairly difficult). This feature is seldom used but it is there for you to use if you wish.

Low and High Byte Data Latch U3

The S-100 bus data bus is 8 bits wide. The IDE drive data bus is 16 bits wide. The drive does not require 16 bit wide data for control so it could be used without the upper 8 bits of data but that would be wasteful of drive space. Scott Christiansen documented a method for converting the bus from 8 to 16 bits and his method was adapted for this design with his XTIDE interface (http://mylinuxisp.com/~jdbaker/oldsite/SmallSys/8bitIDE.html#XTIDE). Others have used this as well, including Robert Doerr, a Heathkit Robot

enthusiast in his H2KIDE Robot drive interface (http://www.theoldrobots.com/hero2k.html), and Jim Hathaway for the Color Computer (CoCoIDE) (http://mylinuxisp.com/~jdbaker/oldsite/SmallSys/8bitIDE.html#CoCo_IDE).

The control for doing this is done in the Altera chip, U13, an EPM7064SLC84. When reading data from the drive, read from the drive at address 008Ch which will give you the low byte, then read the hi byte from the latch, U3, 74LS573, at address 008Dh. Note: Addresses are consecutive so that word-wide computer instructions can be used for higher performance. Data is latched by the signal LATCH_LE. The output is enabled by the signal /LATCH_OE/, feeding hi byte data to buffer U2 and the S100 data bus.

For Write, write the Lo Byte first to the latch at address 0088h, then write the Hi Byte at 0089h. This writes both the Lo Byte and Hi Byte to the drive. Again addresses are consecutive for word-wide instructions. As before, the data is latched with the LATCH_LE signal and the output is enabled by the /LATCH_OE signal. The destination for the latched lo byte data this time though is the IDE data bus.

You could also read the low byte or write the low byte from/to address 80h if you only want 8 bit transfer. This is not recommended as most IDE drives do not support it. You would have to find a really old drive.

NVsRAM (sheet 3 of schematic)

The NVsRAM (U6, BQ4850) is controlled with the following signals:

/RAM_WE NVsRAM write enable. Note: W2 can be used to provide a hard write DISABLE by cutting the trace between the two pads. Then to re-enable write, install a two pin header and install a jumper. We feel that the software is reliable enough that accidental NVsRAM write is unlikely.

/RAM_CE NVsRAM Chip enable

/RAM_RE NVsRAM Output enable (for reading)

W1 is used to configure for a 32-pin or 36-pin NVsRAM. The card comes with the trace in place for a 32-pin NVsRAM. For a 36 pin NVsRAM, cut the trace for 32-pin, install a three pin header and install a jumper on the 36-pin position.

U4, a CD4040 Johnson counter, provides the address counter. The address counter is reset by writing to the Sector Latch 8Eh. The address counter is incremented by reading address 8Fh. The counter is clocked with the INCR/ signal and Cleared with the CLR signal.

Write data to NVsRAM at address 8Fh.
Read data from NVsRAM at address 8Eh.

U5, 74LS573, provides the sector latch. It is loaded by writing the sector value (0 to FFh) to address 8Eh. Each sector is 1024 bytes long. The sector latch is also latched with the CLR signal at the same time the counter is cleared.

The sector latch outputs are always enabled.

The following equates summarize the above:

```
SECTOR_PORT     equ     08Eh; port to specify
NVSRAM sector

READ_PORT       equ     08Eh; read data port

WRITE_PORT      equ     08Fh; write data port

BUMP_PORT       equ     08Fh; reading from
this port increments the flash NVSRAM board
offset pointer
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Note: these equates do not necessarily relate to any specific software. They are examples only.

U6 is the BQ4850 NVsRAM and was described earlier.

Power Regulator (Sheet 3 of schematic)

U20, LM7805, provides the 5v regulated power for the board. The S-100 bus provides approximately 8 volts to the board, from pins 1 and 51, which must be regulated. This is the only operating voltage provided by the board.

Altera Controller

The Altera Controller, U13, EPM7064SLC84, is the heart of the system. It performs the following functions:

1. As previously mentioned, decodes the address lines into the appropriate address located at 008xH. Sixteen address lines are decoded.
2. Controls the NVsRAM for reading and writing.
3. Controls the Byte read/write latch.
4. Controls the IDE Drives
5. Controls all board buffers
6. Debounces the breakout switch and generates the NMI signal for breakout.
7. Ensures that at least two wait states are generated with IDE control for ports 81h – 87h and 8ah. Normally, one or two wait states are selected by a jumper on the Z100 motherboard. The wait states generated here override any jumper there unless more than two are selected.
8. Selects the desired IDE connector J1, J2. Controlled by B0 and B1 at address 008Ch. B0=0 and B1=1 for J1, B0=1 and B1=0 for J2.
9. Drives the two NVsRAM and four IDE drive activity LEDs.

The Altera chip can be programmed while installed on the IDE card via the W3 IDE programming connector. This can be connected to an Altera Byte Blaster compatible programmer. Charles made one using commonly available parts per Altera website instructions.

CAUTION – the Altera chip can be damaged doing this under some circumstances. Use care that I/O pin definition is compatible with the programming change being contemplated. A separate article describing programming in more detail will be available.

Breakout Switch

A breakout switch is located in the extreme upper right corner of the IDE Controller Board to generate an NMI interrupt signal for breakout. The switch can be pressed at any time to exit to the monitor-ROM hand prompt. To return to the application in progress, at the hand prompt, press {Go and {RETURN} {RETURN}. The right-most pins on the LED connector can also be connected to another, optional breakout switch that you may locate anywhere in the Z-100 case.

LEDs

The IDE Controller Board comes standard with an LED assembly mounted on the LED connector to provide indications for NVsRAM and IDE drive activity. This assembly can be removed and replaced by your own assembly to mount a bank of LED's somewhere on the front panel. These are very handy for software debugging and discerning proper IDE card activity.

Altera Chip to IDE Schematic Pinout

Pin	Altera Pin Name/Usage	Schematic Name	Dir.	Pin	Altera Pin Name/Usage	Schematic Name	Dir.
1	RESET/_75	RESET/_75	input	43	VCCINT	VCCINT	power
2	pSYNC_76	pSYNC_76	input	44	J2_25_IOR/	J2_25_IOR/	output
3	VCCINT	VCCINT	power	45	J1_38_DS1/	J1_38_DS1/	output
4	pWR/_77	pWR/_77	input	46	J2_23_IOW/	J2_23_IOW/	output
5	pDBIN_78	pDBIN_78	input	47	GND	GND	gnd
6	A[5]	A[5]_29	input	48	J1_37_DS0/	J1_37_DS0/	output
7	GND	GND	gnd	49	J1_35_A0	J1_35_A0/	output
8	A[0]	A[0] _79	input	50	J1_36_A2	J1_36_A2	output
9	A[4]	A[4]_30	input	51	J1_25_IOR/	J1_25_IOR/	output
10	A[3]	A[3] _31	input	52	J1_33_A1	J1_33_A1	output
11	A[1]	A[1]_80	input	53	VCCIO	VCCIO	power
12	A[2]	A[2]_81	input	54	D[2]	D[2]/DD10	input
13	VCCIO	VCCIO	power	55	J1_23_IOW/	J1_23_IOW/	output
14	TDI	#TDI	input	56	D[1]	D[1]/DD9	input
15	A[15]	A[15] _32	input	57	[D4]	[D4]/DD12	input
16	A[12]	A[12]_33	input	58	D[0]	D[0]/ DD8	input
17	A[6]	A[6]_82	input	59	GND	GND	gnd
18	A[7]	A[7]_83	input	60	DIR	DIR	output
19	GND	GND	gnd	61	J1_OE/	J1_OE/	output
20	A[8]	A[8]_84	input	62	TCK	#TCK	input
21	A[9]	A[9]_34	input	63	NVsRAM_CE/	NVsRAM_CE/	output
22	A[13]	A[13_85	input	64	NVsRAM_OE/	NVsRAM_OE/	output
23	TMS	#TMS	input	65	NVsRAM_WE/	NVsRAM_WE/	output
24	A[10]	A[10]_37	input	66	VCCIO	VCCIO	power
25	A[14]	A[14]_86	input	67	J2_OE/	J2_OE/	output
26	VCCIO	VCCIO	power	68	IDE_RESET_1/	IDE_RESET_1/	output
27	A[11]	A[11]_87	input	69	LATCH_LE	LATCH_LE	output
28	sINP_46	sINP_46	input	70	LED_J2_SLAVE	LED_J2_SLAVE	output
29	sOUT_45	sOUT_45	input	71	TDO	#TDO	output
30	I/O_Write_OE/	I/O_Write_OE/	output	72	GND	GND	gnd
31	I/O_Read_OE/	I/O_Read_OE/	output	73	LED_J2_MASTER	LED_J2_MASTER	output
32	GND	GND	gnd	74	LED_J1_MASTER	LED_J1_MASTER	output
33	CLR	CLR_RST_LE	output	75	NVsRAM_RD_LED	NVsRAM_RD_LED	output
34	LATCH_OE/	/LATCH_OE	output	76	LED_J1_SLAVE	LED_J1_SLAVE	output
35	J2_38_DS1/	J2_38_DS1/	output	77	BREAKOUT	BREAKOUT	input
36	INCR4040_CLK	INCR4040CLK	output	78	VCCIO	VCCIO	power
37	J2_37_DS0/	J2_37_DS0/	output	79	NMI_12	NMI_12	output
38	VCCIO	VCCIO	power	80	NVsRAM_WR_LED	NVsRAM_WR_LED	output
39	J2_35_A0	J2_35_A0	output	81	RDY_72	RDY_72	bidir
40	J2_36_A2	J2_36_A2	output	82	GND	GND	gnd
41	J2_33_A1	J2_33_A1	output	83	PHI_24	PHI_24	input
42	GND	GND	gnd	84	pSTVAL/_25	pSTVAL/_25	input

Note:

- A "/" character in the signal name indicates the signal is active when low.
- A "#" character in the signal name indicates the signal is used for programming the Altera chip and has no function in the IDE interface.

It is suggested that you obtain a copy of the FPGA socket diagram which will show the pinout translation from the IDE Controller chip to the PC board. It is rather tricky. One source for this drawing would be at Mill-Max:

http://www.mill-max.com/images/products/application_notes/940FP.pdf

Go to the 84 pin socket. It will be very helpful if you need to troubleshoot the card.